plurality of memory cells are consecutively arranged and serve as word lines. FIG. 4A is the section in the direction parallel to a direction of the word line.

Replace the paragraph starting on page 2, line 10 with the following text:

The silicon oxide layer 5a, on the side of the floating gate 4, of the ONO layer 5, if a layer thickness thereof is 5 – 6nm, works as a Fowler-Nordheim type tunnel current conductive mechanism, wherein the electric current flowing with a low electric field is extremely small. Further, a barrier height of the silicon oxide layer 5a with respect to silicon is as high as 3.2 eV. Accordingly, if the silicon oxide layer 5 has no defects and there is no electric field enhancement effect based on a two-dimensional configuration of the floating gate 4, only the silicon oxide layer 5a must be capable of sufficiently retaining the electrons for a long time. In fact, however, there exist defects and the two-dimensional electric field enhancement effect, and hence the ONO layer is used.

IN THE CLAIMS:

Please amend the claims as follows:

Please replace the text of claim 1 with the following text:

1. A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on the semiconductor substrate, and a control gate provided through an inter-layer insulating layer on the floating gate, wherein the inter-insulating layer includes:

a silicon oxide layer contiguous to the floating gate;

a first silicon nitride layer provided by a CVD method on the silicon oxide layer; and

a second silicon nitride layer provided on the first silicon nitride layer and having a lower trap density than that of said the silicon nitride layer.

Please replace the text of claim 2 with the following text: